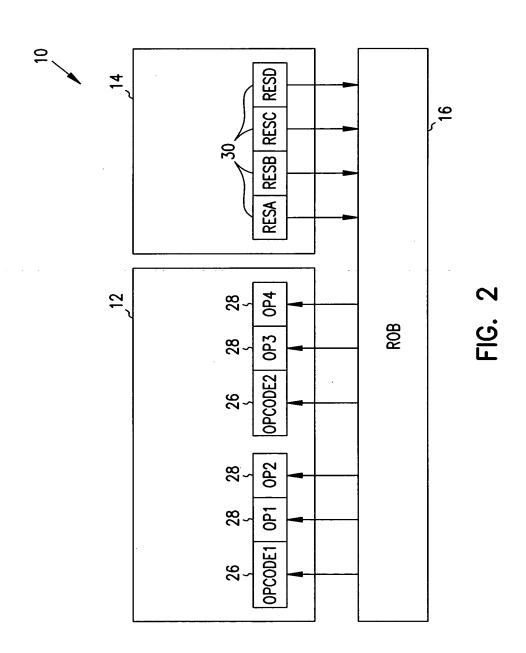


FIG. 1



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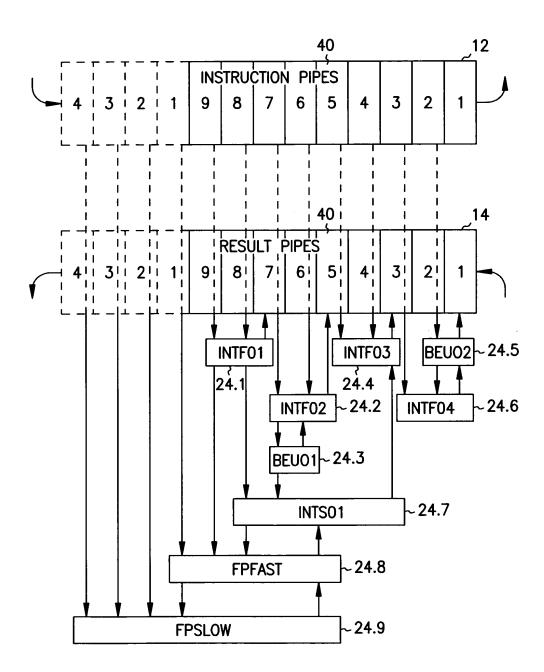


FIG. 3

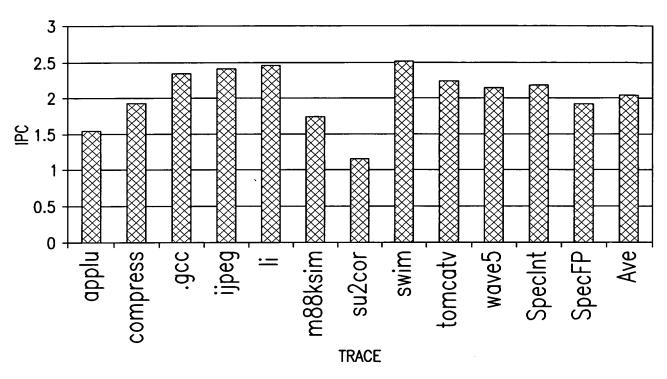
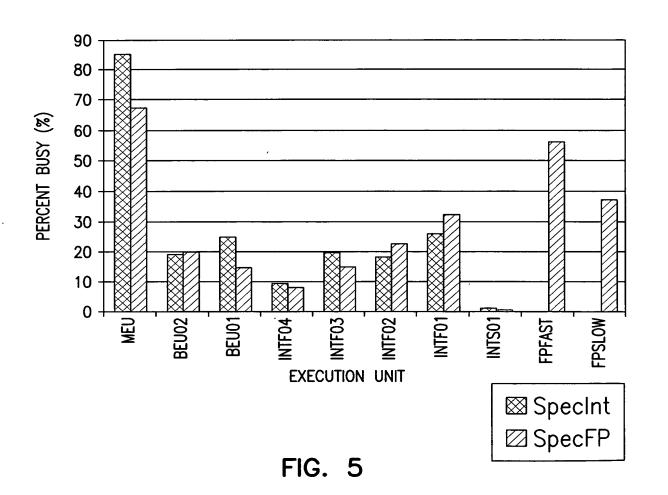
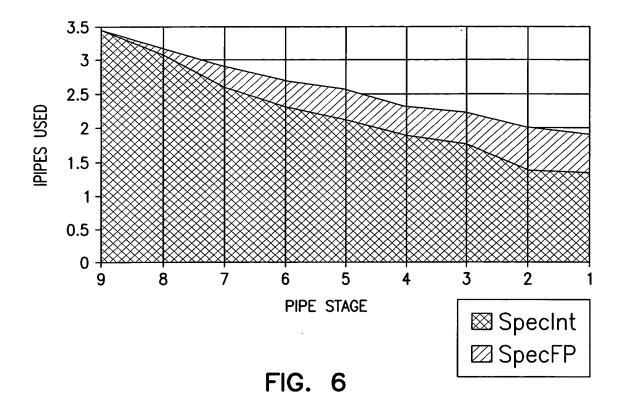
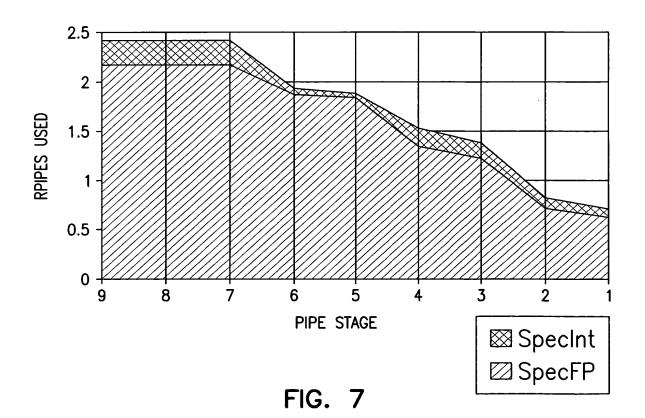


FIG. 4

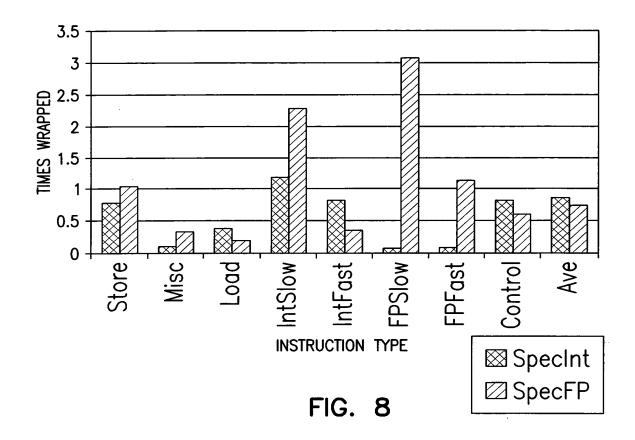


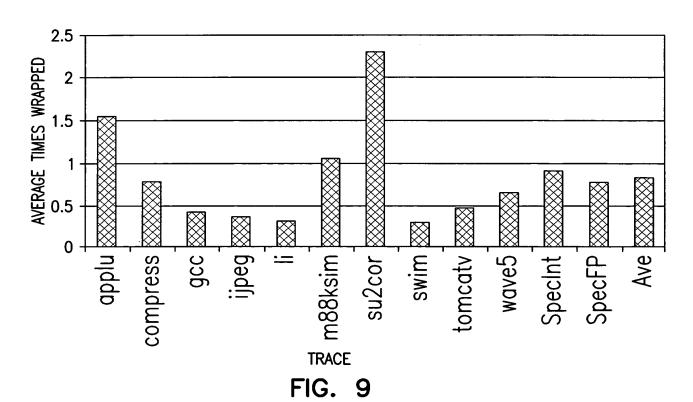
DOCKET NO.: 884.002US6





DOCKET NO.: 884.002US6





TITLE: NON-STALLING CIRCULAR COUNTERFLOW PIPELINE PROCESSOR WITH REORDER BUFFER

INVENTORS NAME: Kenneth J. Janik et al. DOCKET NO.: 884.002US6

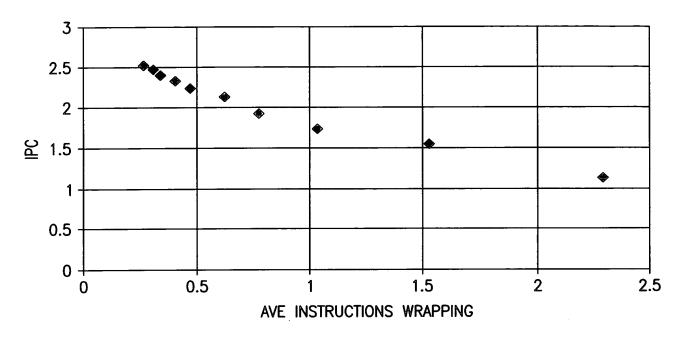


FIG. 10

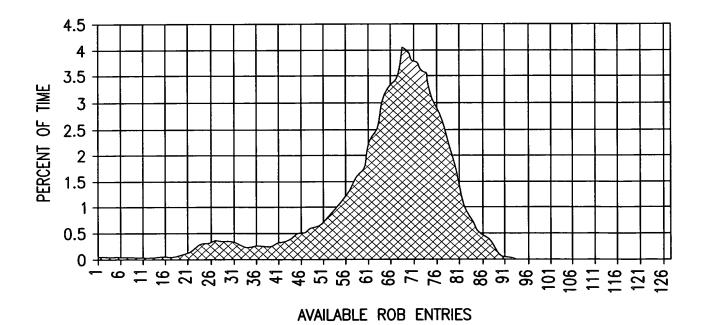


FIG. 11

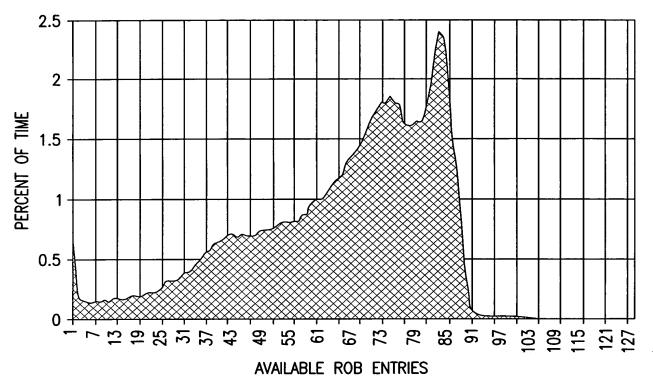
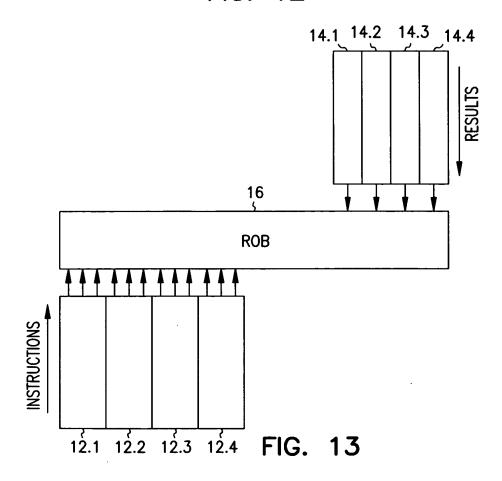


FIG. 12



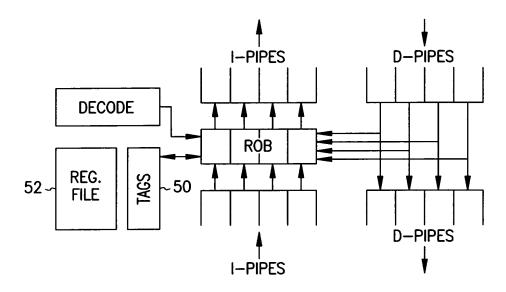
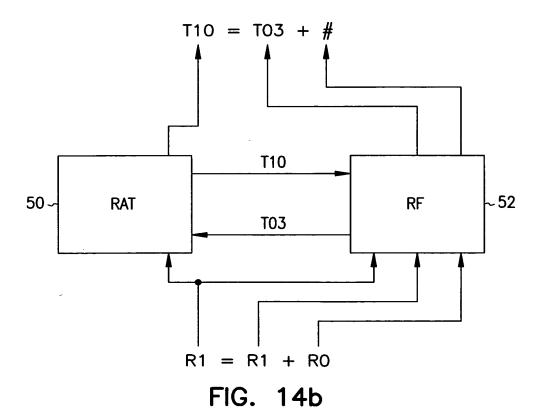


FIG. 14a



TITLE: NON-STALLING CIRCULAR COUNTERFLOW PIPELINE PROCESSOR WITH REORDER BUFFER

INVENTORS NAME: Kenneth J. Janik et al. DOCKET NO.: 884.002US6

	PIPE	REGISTER	LAST			VALID	ALIAS	
HEAD ── 0	0	XX	XX	~50	0	1	XX	<b>]∼52</b>
1	1	XX	XX		1	0	03	
2	0	XX	XX		2	1	XX	
TAIL — 3	0	R1	03		3	1	XX	
		(RAT)				(	(RF)	_

FIG. 15a

	PIPE	REGISTER	LAST			VALID	ALIAS	
0	1	R1	03	~50	0	1	XX	~52
HEAD — 1	1	XX	XX		1	0	10	
2	0	XX	XX		2	1	XX	
TAIL — 3	0	R1	03		3	1	XX	
		(RAT)				(	RF)	_

FIG. 15b

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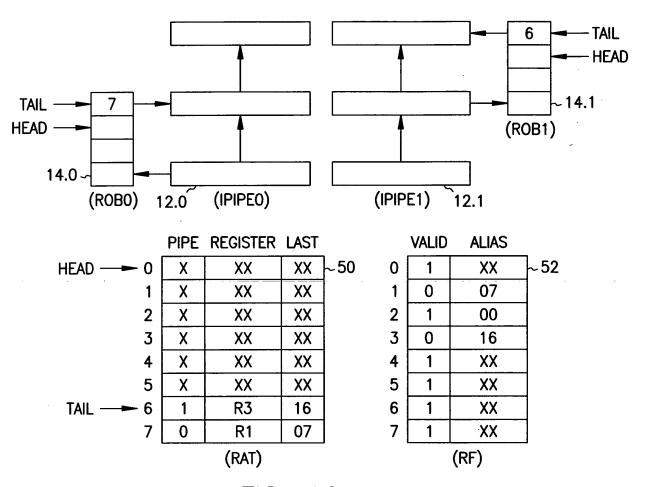


FIG. 16a

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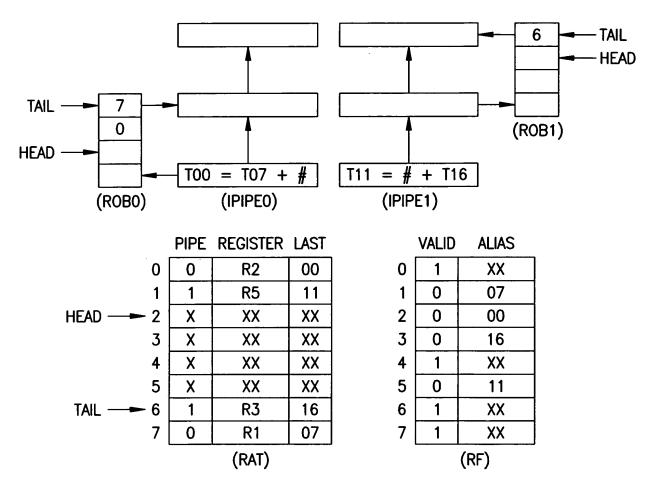


FIG. 16b

TITLE: NON-STALLING CIRCULAR COUNTERFLOW PIPELINE PROCESSOR WITH REORDER BUFFER

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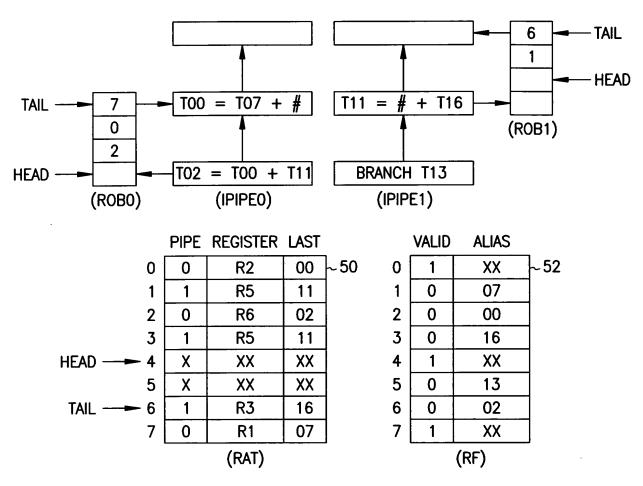


FIG. 16c

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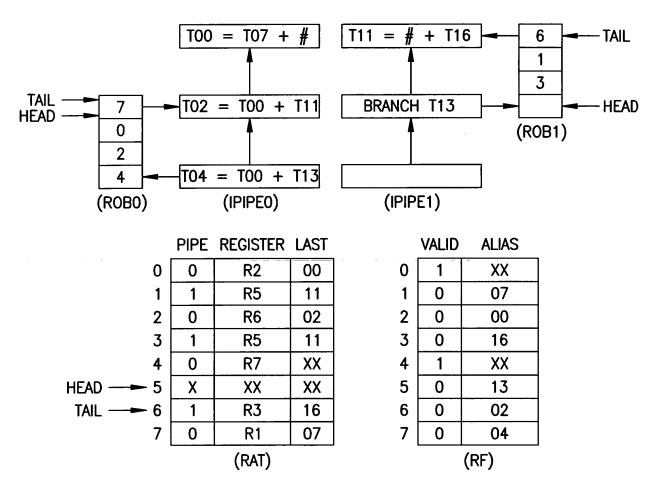


FIG. 16d

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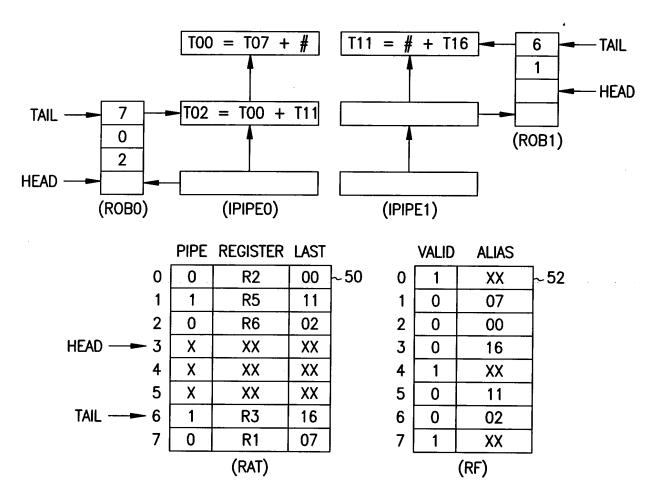


FIG. 16e

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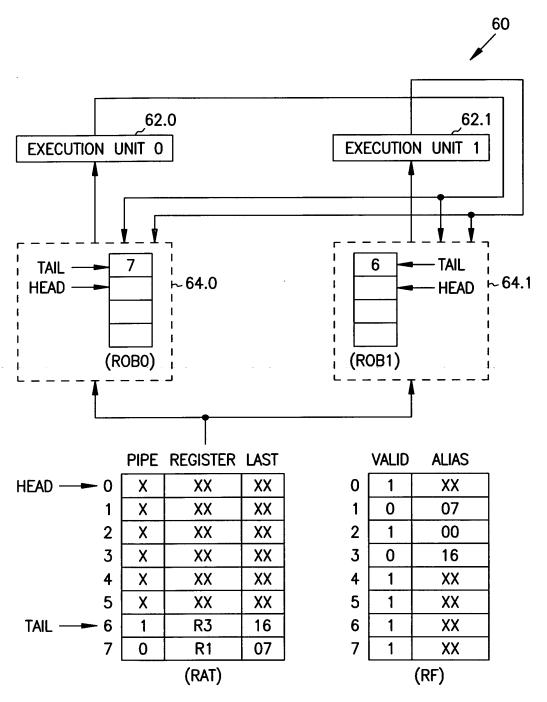


FIG. 17

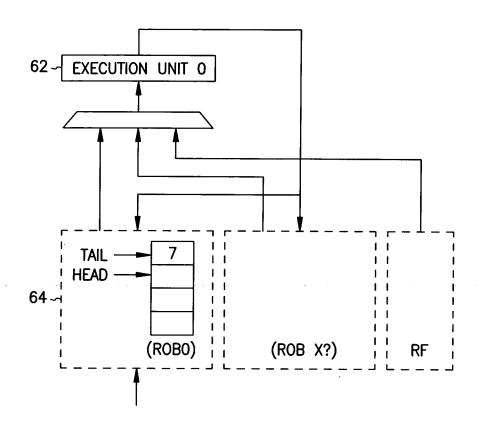
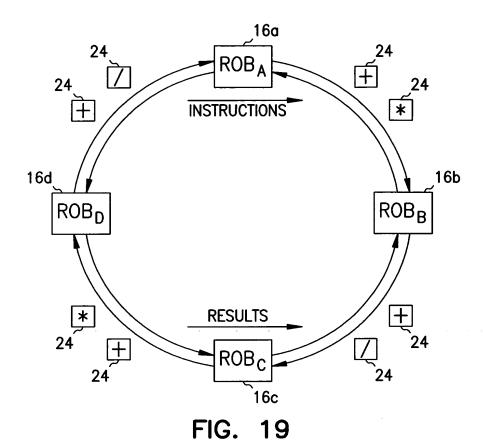
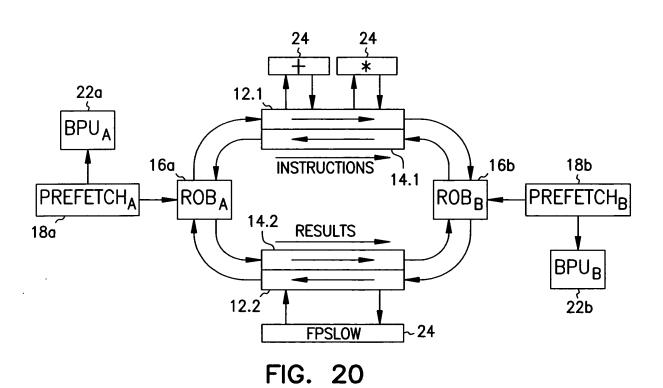


FIG. 18





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	10	Ш	T1 T2 T3 T4 T5	13	14	15	16	41	T8	T9
LOAD R1, X	V/P (CORRECT)						eV/NP	RET		
LOAD R9, Y	V/P (INCORRECT)						eV/NP	RET		
ADD R2, R1, R2			eV/P				:	N/N	RET	
ADD R3, R4, R2					eV/P				V/NP RET	RET
ADD R8, R9, R4				eV/P				eV/NP		RET
ADD R7, R8, R4						eV/P			dN//a	RET
ADD R5, R5, R5		eV/NP								RET
•••										

FIG. 21